What is claimed is:

1. A microcontroller, comprising:

a clock input pin, wherein an input signal from the external circuit is inputted;

a clock generating means for generating a clock signal by receiving a signal from the clock input pin;

a clock output pin for receiving an output signal of the clock generating means and outputting the output signal;

a first switch for transmitting an internal signal of a microcontroller to the clock output pin for using the clock output pin is in a system mode; and

a second switch, which is enabled when the clock generating means is operated in the clock generation mode and disabled when the microcontroller is operated in the system mode.

2. The apparatus as recited in claim 1, wherein the second switch includes a plurality of switches connected in parallel.

3. The apparatus as recited in claim 2, further comprising a control means for selectively controlling each of switches depending on a clock signal of the clock input pin.

4. The apparatus as recited in claim 1, further comprising a control means for selectively enabling first and second switches classified by modes.

5. The apparatus as recited in claim 2, further comprising a control means for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.

6. The apparatus as recited in claim 1, wherein the clock generating means includes:

an inverter for amplifying an input signal as a full-swing to generate a clock signal; and

a resistor, which is connected to input and output terminals of the inverter.

7. A system having a microcontroller, comprising:

a clock input pin for receiving an input signal;

a first clock generating means for receiving a signal from the clock input pin to generate a clock signal;

a first switch for transmitting an internal signal of a microcontroller to the clock output pin for using the clock output pin is in a system mode;

a second switch, which is enabled when the clock generating means is operated in the clock generation mode and disabled when the microcontroller is operated in the system mode; and

a second clock generating means for providing a clock signal to the microcontroller through the clock input pin in a system mode.

8. The apparatus as recited in claim 7, wherein the second switch includes a plurality of switches connected in parallel.

9. The apparatus as recited in claim 8, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on a frequency of a clock signal of the clock input pin.

10.The apparatus as recited in claim 7, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.

11.The apparatus as recited in claim 8, further comprising a control means, which is placed in either inside or outside of the microcontroller, for selectively controlling each of switches depending on the frequency of the clock signal of the clock input pin and for selectively controlling each of switches depending on a clock signal of the clock input pin and selectively enabling first and second switches classified by modes.